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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Wood et al.

Patent No.: 6,036,872

Examiner: N. Nguyen

Serial No.: 09/052,645

Issued: March 14, 2000

Group Art Unit: 1763

Filed: March 31, 1998

For: METHOD OF MAKING A WAFER-PAIR HAVING SEALED CHAMBERS

Docket No.: 1100.1138101 (H16-17400)

PRELIMINARY AMENDMENT

BOX REISSUE

U.S. Patent and Trademark Office P.O. Box 2327 Arlington, VA 22202

CERTIFICATE UNDER 37 C.F.R. 1.10: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, "Express Mail Post Office to Addressee" having an Express Mail mailing label number of EL901546446US, in an envelope addressed to:

U.S. Patent and Trademark Office, P.O. Box 2327, Arlington, VA 22202

on this Brd day of December 2001.

Jolene Alger

Sir:

Please amend the above-captioned application as follows:

In the Claims

Please add newly presented claims 25-55 as follows:

25. A method for making a wafer-pair having deposited layer plugged sealed chambers, comprising:

growing a thermal layer on a first side of a first wafer;

depositing a nitride layer on the thermal layer;

depositing, patterning and removing portions of first metal layer on the nitride

layer for a plurality of devices;

depositing, patterning and removing portions of a second metal layer on the nitride and first metal layers for the plurality of devices;

of the first wafer and from a second side of the first wafer to make a plurality of pumpout ports through the first wafer and layers on the first wafer;

masking and removing material from a first side of a second wafer to form a plurality of recesses in the first side of the second wafer;

forming a sealing ring on the first side of the second wafer around each of the plurality of recesses; and

positioning the first side of the first wafer next to the first side of the second wafer; and wherein:

each sealing ring is in contact with at least one of the layers on the first side of the first wafer;

each recess of the plurality of recesses results in a chamber containing at least one device of the plurality of devices;

each sealing ring encloses at least one pump-out port of the plurality of pump-out ports; and

the first and second wafers are effectively a bonded together set of wafers.

26. The method of claim 25, further comprising:

placing the set of wafers in an environment of a vacuum wherein a vacuum occurs in each chamber via the at least one pump-out port; and

depositing a layer of material on the second side of the first wafer and the plurality of pump-out ports on the second side of the first wafer, wherein each chamber is sealed from the environment.

- 27. The method of claim 26, further comprising baking out the set of wafers prior to depositing the layer of material on the second side of the first wafer and the plurality of pump-out ports on the second side of the first wafer.
- 28. The method of claim 27, further comprising coating the second wafer with antireflection material.
- 29. The method of claim 28, wherein the second wafer is made from a material that is at least substantially transparent to light in the infrared spectrum.
- 30. The method of claim 29, wherein the plurality of devices comprise thermoelectric detectors.
- 31. The method of claim 30, wherein the plurality of devices comprise bolometers.
- 32. A method for making a wafer-pair having at least one deposited layer plugged sealed chamber, comprising:

growing a first thermal layer on a first side of a first wafer;

depositing a nitride layer on the first thermal layer;

depositing and patterning a first metal layer on the nitride layer for at least one device;

depositing and patterning a second metal layer on the nitride layer and the first metal layer for the at least one device;

patterning and removing material from the first wafer and layers on the first side
of the first wafer and from a second side of the first wafer to make a pump-out port
through the first wafer and the layers on the first wafer;

masking and removing material from a first side of a second wafer, to form a recess in the first side of the second wafer;

forming a sealing ring on the first side of the second wafer around the recess;

positioning the first side of the first wafer next to the first side of the second

wafer; and

wherein:

the sealing ring is in contact with at least one of the layers on the first side of the first wafer;

the at least one device is within the recess resulting in a chamber containing the at least one device;

the pump-out port is within the sealing ring; and the first and second wafers are effectively a bonded together set of wafers.

33. The method of claim 32, further comprising:

placing the bonded together set of wafers in an environment of a vacuum wherein a vacuum occurs in the chamber via the pump-out port; and

depositing a layer of material on the second side of the first wafer and the pumpout port on the second side of the first wafer, wherein the chamber is sealed from the environment.

- 34. The method of claim 33, further comprising baking out the bonded together set of wafers prior to depositing the layer of material on the second side of the first wafer and the pump-out port on the second side of the first wafer.
 - 35. The method of claim 34, wherein the at least one device is a detector.
- 36. The method of claim 35, wherein the at least one device is a thermoelectric detector.
 - 37. The method of claim 34, wherein the at least one device is an emitter.
- 38. A method for making a wafer-pair having sealed chambers, comprising:

 patterning and removing material from a first wafer to make a plurality of pumpout ports through the first wafer;

masking and removing material from a first side of a second wafer to form a plurality of recesses in the first side of the second wafer;

forming a sealing ring on a first side of the first wafer or the first side of the second wafer such that the sealing ring extends around each of the plurality of recesses; and

positioning the first side of the first wafer next to the first side of the second wafer; and

wherein:

each sealing ring is in contact with the first side of the first wafer and the first side of the second wafer

each recess of the plurality of recesses results in a chamber;

each sealing ring encloses at least one pump-out port of the plurality of pump-out

ports; and

the first and second wafers are effectively a bonded together set of wafers.

39. The method of claim 38, further comprising:

placing the set of wafers in an environment of a vacuum wherein a vacuum occurs in each chamber via a pump-out port; and

depositing a layer of material on a second side of the first wafer to seal the plurality of pump-out out ports from the second side of the first wafer, wherein each chamber is sealed from the environment.

40. The method of claim 39, further comprising baking out the set of wafers prior to depositing the layer of material on the second side of the first wafer.

- 41. The method of claim 40, wherein the set of wafers is cut into a plurality of chips wherein each chip has one or more sealed chambers.
- 42. The method of claim 40, wherein the one or more sealed chambers contains one or more devices.

43. The method of claim 38, further comprising:

placing the set of wafers in an environment of a gas wherein the gas enters each chamber via a pump-out port; and

depositing a layer of material on a second side of the first wafer to seal the plurality of pump-out out ports from the second side of the first wafer, wherein each chamber is sealed from an ambient environment.

44. A method for making a wafer-pair with a sealed chamber therebetween, comprising:

providing a first wafer and a second wafer;

forming one or more pump-out ports through the first wafer;

positioning a first side of the first wafer next to a first side of the second wafer with a sealing ring therebetween, the first wafer, the second wafer and the sealing ring forming a chamber, with the pump-out port of the first wafer in fluid communication with the chamber; and

plugging the pump out port to seal the chamber.

- 45. A method according to claim 44 further comprising the step of:

 making a recess in the first side of the first wafer and/or the first side of the
 second wafer, wherein the recess is in registration with the chamber.
- 46. A method according to claim 44 further comprising the step of:

 providing one or more devices in or on the first side of the first wafer and/or the first side of the second wafer before the positioning step.
- 47. A method according to claim 46 wherein the one or more devices are in registration with the chamber.
- 48. A method for making a wafer-pair with a sealed chamber therebetween, comprising:

providing a first wafer and a second wafer;

forming one or more pump-out ports through the first wafer;

making a recess in a first side of the first wafer and/or a first side of the second wafer;

positioning the first side of the first wafer next to the first side of the second wafer, the first wafer and the second wafer forming a chamber that is at least partially defined by the recess, with the pump-out port of the first wafer in fluid communication with the chamber; and

plugging the pump out port to seal the chamber.

49. A method for making a wafer-pair with a sealed chamber therebetween, comprising:

providing a first wafer having a first side, with one or more bond pads on the first side;

providing a second wafer;

forming one or more bond-pad holes through the second wafer;

positioning the first side of the first wafer next to a first side of the second wafer with a sealing ring therebetween; the first wafer, the second wafer and the sealing ring forming a chamber, the first wafer and second wafer being aligned so that the bond-pad holes are in registration with the one or more bond pads on the first wafer; and the first and second wafers are effectively a bonded together set of wafers.

50. A bonded wafer pair, comprising:

a first wafer;

a second wafer;

the first wafer having one or more pump-out ports through the first wafer;

the first side of the first wafer bonded to a first side of the second wafer via a

sealing ring; the first wafer, the second wafer and the sealing ring forming a chamber,

with the pump-out port of the first wafer in fluid communication with the chamber; and
a plug for plugging the pump out port.

- 51. A bonded wafer pair according to claim 50 further comprising a recess in the first side of the first wafer and/or the first side of the second wafer, wherein the recess is in registration with the chamber.
- 52. A bonded wafer pair according to claim 50 further comprising one or more devices in or on the first side of the first wafer and/or the first side of the second wafer.
- 53. A bonded wafer pair according to claim 52 wherein the one or more devices are in registration with the chamber.
- 54. A bonded wafer pair having a sealed chamber, comprising:

 a first wafer;

 a second wafer bonded to the first wafer;

 one or more pump-out ports through the first wafer;

 a recess in a first side of the first wafer and/or a first side of the second wafer;

 the first wafer and the second wafer forming a chamber that includes the recess,

 with the pump-out port of the first wafer in fluid communication with the chamber; and
- one or more plugs for plugging the one or more pump out ports to seal the chamber.
 - 55. A bonded wafer pair, comprising:

 a first wafer having a first side, with one or more bond pads on the first side;

a second wafer, with one or more bond-pad holes through the second wafer;

the first side of the first wafer bonded to a first side of the second wafer with a sealing ring therebetween, the first wafer and second wafer being aligned so that the bond-pad holes are in registration with the one or more bond pads on the first wafer; and the first wafer, the second wafer and the sealing ring forming a chamber.

Remarks

Applicants request that the preceding claim amendments be made of record and fully considered before the first Office Action on the merits. Any inquiry regarding this matter may be directed to the undersigned representative at (612) 677-9050.

Respectfully submitted,

R. Andrew Wood et al.

By their attorney,

Date: December 3, 2001

Brian/N. Tufte/Reg. No. 38,638

CROMPTON, SEAGER & TUFTE, LLC

331 Second Avenue South, Suite 895

Minneapolis, Minnesota 55401-2246

Telephone:

(612) 677-9050

Facsimile:

(612) 359-9349

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Wood et al.

Patent No.: 6,036,872

Examiner: N. Nguyen

Serial No.: 09/052,645

Issued: March 14, 2000 Filed: March 31, 1998 Group Art Unit: 1763

For: METHOD OF MAKING A WAFER-PAIR HAVING SEALED CHAMBERS

Docket No.: 1100.1138101 (H16-17400)

STATUS OF CLAIMS AND SUPPORT FOR CLAIM CHANGES (37 CFR 1.173(C))

BOX REISSUE

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CERTIFICATE UNDER 37 C.F.R. 1.10: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, "Express Mail Post Office to Addressee" having an Express Mail mailing label number of <u>EL901546446US</u>, in an envelope addressed to: U.S. Patent and Trademark Office, P.O. Box 2327, Arlington, VA 22202

on this 3rd day of December 2001.

Jolene Alger

Sir:

In accordance with 37 CFR §1.173(c)): "Whenever there is an amendment to the claims pursuant to paragraph (b) of this section, there must also be supplied, on pages separate from the pages containing the changes, the status (i.e., pending or cancelled), as of the date of the amendment, of all patent claims and of all added claims, and an

explanation of the support in the disclosure of the patent for the changes made to the claims."

The status of the claims as a result of the amendment submitted herewith is:

Claims 25-55 have been added.

The support in the disclosure of the patent for the changes made to the claims and for the claims added is as follows:

Claim #	Claim Phrase	Examples of Locations in
25	A method for making a wafer-pair having deposited layer plugged sealed chambers, comprising:	Specification that disclose the claimed element. Column 2 lines 10-12: "FIGS. 1a, 1b and 2 show an illustration of a device 10 having a vacuum pump-out port 11 and a deposited plug final vacuum seal 12."
	growing a thermal layer on a first side of a first wafer;	Column 2 lines 49-51: "A 1000 angstroms of a thermal SiO ₂ layer 24 is grown on the front of wafer 13 in FIG. 4B."
r	depositing a nitride layer on the thermal layer;	Column 2 lines 51-53: "A layer 25 of 2000 angstroms of Si_3N_4 (bottom bridge nitride) is deposited on layer 24 in FIG. 4c."
	depositing, patterning and removing portions of first metal layer on the nitride layer for a plurality of devices;	Column 2 lines 53-56: "The first metal NiFe (60:40) of a thermocouple is deposited as a 1100 angstrom layer 26 on layer 25 and then first metal layer 26 is patterned with a first mask by ion milling resulting in the layout of FIG. 4d."
	depositing, patterning and removing portions of a second metal layer on the nitride and first metal layers for the plurality of devices;	Column 2 lines 57-60: "For the second metal of the thermocouple detectors, a thousand angstrom layer 27 of chromium is deposited on layers 25 and 26. Layer 27 in FIG. 4e is patterned with a second mask by ion milling and wet etching."
*	patterning and removing material from the first wafer and layers on the first side of the first wafer and from a second side of the first wafer to make a plurality of pump-out ports through the first wafer and layers on the first wafer;	"Plasma etched vias 32 in FIG 4i for the final etch are patterned and cut with the use of a fifth mask." (Column 2 line 68 to column 3 line 1). "Plasma etched pump-out port vias 11 are patterned and cut on layers 23b and 23a of the back of wafer 13 in FIG 4k. There is a KOH etch of the backside of wafer 13 through 90 percent of wafer 13 for port 11 in FIG 4l. Port 11 is completed with an etch through via 32 to the front of wafer 13 as shown in FIG 4m." (Column 3 lines 6-11).

masking and removing material from a first side of a second wafer to form a plurality of recesses in the first side of the second wafer;	"Pattern and cut via 35 by plasma etching on outside layers 36a and 36b and recess 16 on inside layer 37b of Si ₃ N ₄ in FIG. 5b." (Column 3 lines 29-31). "Wafer 14 is removed from the etching fixture and hole 16 is cleared of remaining SiO ₂ layer 37a in FIG. 5d by buffered oxide etch." (Column 3 lines 35-37). "Nitride and oxide mask layers 36a, 36b, 37a, and 37b are stripped from wafer 14." (Column 3 lines 39-41).
forming a sealing ring on the first side of the second wafer around each of the plurality of recesses; and	"A solder ring pattern is applied to the inside surface encircling recess 16, by using a laminated Riston process for lift-off. Five hundred angstroms of Ti, 2000 angstroms of Ni and 500 angstroms of Au of adhesion metals 39 are deposited in an E-beam evaporator. A five micron layer 40 of InPb (10:90) solder is deposited onto adhesion metals 39 in the thermal evaporator. The Riston mask is lifted off and the field SiO.sub.2 in BOE etched off resulting in solder ring 18 in FIG. 5f." (Column 3 lines 41-50).
positioning the first side of the first wafer next to the first side of the second wafer; and wherein:	"Wafers 13 and 14 of FIG. 6a are aligned in a bonding cassette using 0.002 inch spacers between the wafers." (Column 3 lines 58-60).
each sealing ring is in contact with at least one of the layers on the first side of the first wafer;	"Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure." (Column 3 lines 62-63)
each recess of the plurality of recesses results in a chamber containing at least one device of the plurality of devices;	In describing Figures 1a, 1b, and 2, "Cavity 16 is the chamber that contains an array 17 of detectors on the surface of wafer 13 and detects radiation which may come through an anti-reflective coated silicon window of top cap 14." (Column 2 lines 17-20.) Further, a plurality of such recesses are shown in Figure 3: "FIG. 3 shows a wafer 20 having multiple chips 10 having a wafer-to-wafer sealing of the same material for multiple cavities." (Column 2 lines 28-30). Further, in describing a nearly finished product, "Wafer 20 may be cut into individual chips 10, each having its own sealed chamber 16 enclosing detectors 17." (Column 4 lines 15-17)
each sealing ring encloses at least one pump-out port of the plurality of pump-out ports; and	As shown in Figures 1a and 1b. As noted in Column 2 lines 3 0-31, "Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11." Column 3 lines 42-50 note that a solder ring pattern (a sealing ring) encircles the recess. Column 4 lines 15-17 notes that each chip has its own sealed chamber.
the first and second wafers are effectively a	"Wafers 13 and 14 are adhered together at a solder seal ring 15." (Column 2 lines 15-16).

bonded together set of wafers.	"The present wafers 13 and 14, after bonding and sealing, may be sawed into individual chips without breakage since the sealed top cap protects the fragile microstructure devices 17. Further, the plug will not be disturbed since it is a deposited layer 12 rather than some dislodgable solder ball or plug." (Column 2 lines 37-42) "The aligned wafer pair is put in a vacuum press which is pumped to a good vacuum with a turbo pump. Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for five minutes. Then wafers 13 and 14 are cooled down to room temperature, and the vacuum chamber is vented. The aligned wafer pair is put in a vacuum press which is pumped to a good vacuum with a turbo pump. Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this
	achieved temperature and pressure for five minutes. Then wafers 13 and 14 are cooled down to room temperature, and the vacuum chamber is vented." (Column 3 lines 60-68).
	"Bonded wafer pair 13 and 14" (Column 4 line 1) "Then wafers 13 and 14, combined as wafer 20, may be removed from the vacuum environment." (Column 4 lines 13-15).
The method of claim 25, further comprising: placing the set of wafers in an environment of a vacuum wherein a vacuum occurs in each chamber via the at least one pump-out port; and	"Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11. Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 30-34). "Wafer pair 13 and 14 is put into a thermal evaporator system; and a bake out of the wafer pair at 250 degrees C. is preferred for four hours under a vacuum. The wafer pair 13 and 14 is cooled down but the environment about the wafer pair is kept at the desired vacuum. Twenty microns of InPb (50:50) 12 is deposited onto the backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20 scale, a plurality of ports 11 in a plurality of chips are plugged. Then wafers 13 and 14, combined as wafer 20, may be removed from the vacuum environment. Wafer 20
depositing a layer of	may be cut into individual chips 10, each having its own sealed chamber 16 enclosing detectors 17." (Column 4 lines 4-17).
material on the second	"Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby

side of the first wafer and the plurality of pump-out ports on the second side of the first wafer, wherein each chamber is sealed from the environment. 27 The method of claim 26, further comprising baking out the set of wafers prior to depositing the layer of close ports 11 and seal chambers 16 closed with a vacuum in chambers 31-34). "Twenty microns of InPb (50:50) 12 is deposited onto backside of detector wafer 13 to plug port 11 in FIG. 6c, to so vacuum chamber 16 of wafer pair 13 and 14. On the wafer scale, a plurality of ports 11 in a plurality of chips are plugge (Column 4 lines 9-13). "Cavities 16 can be baked out and outgassed since expectation of metal 12 is applied to the wafer surface having ports 11 and thereby close ports 11 and so chambers 16 closed with a vacuum in the chambers." (Column 4 lines 9-13).
material on the second side of the first wafer and the plurality of 2 lines 30-34). "Wafer pair 13 and 14 is put into a thermal evapora system; and a bake out of the wafer pair at 250 degrees C.
pump-out ports on the second side of the first wafer. preferred for four hours under a vacuum." (Column 4 lines 4-7)
The method of claim 27, further comprising coating the second wafer with antireflection material. "radiation which may come through an anti-reflectic coated silicon window of top cap 14." (Column 2 lines 19-20) "Antireflective coating 38 is applied to wafer 14." (Column 2 lines 19-20)
The method of claim 28, wherein the second wafer is made from a material that is at least substantially transparent to light in the infrared spectrum "Further variations on this theme include top cap wafer composed of Germanium for better IR transmission or ZnSe for application specific optical bandpa behavior." (Column 4 lines 18-22).
The method of claim 29, wherein the plurality of devices comprise thermoelectric detectors thermoelectric detectors "Each cavity, chamber or volume may contain detector such as thermoelectric detectors, devices, bolometers, or may contain emitters." (Column 1 lines 56-58).
The method of claim 30, wherein the plurality of devices comprise bolometers "Each cavity, chamber or volume may contain detector such as thermoelectric detectors, devices, bolometers, or may contain emitters." (Column 1 lines 56-58). "Detector wafer 13 may have infrared bolometer arrays with readout electronics integrated into the wafer." (Column 4 lines 26-28).
A method for making a Column 2 lines 10-12: "FIGS. 1a, 1b and 2 show a

	wafer-pair having at least one deposited layer plugged sealed chamber, comprising:	illustration of a device 10 having a vacuum pump-out port 11 and a deposited plug final vacuum seal 12."
	growing a first thermal layer on a first side of a first wafer;	Column 2 lines 49-51: "A 1000 angstroms of a thermal SiO ₂ layer 24 is grown on the front of wafer 13 in FIG. 4B."
	depositing a nitride layer on the first thermal layer;	Column 2 lines 51-53: "A layer 25 of 2000 angstroms of Si ₃ N ₄ (bottom bridge nitride) is deposited on layer 24 in FIG. 4c."
	depositing and patterning a first metal layer on the nitride layer for at least one device;	Column 2 lines 53-56: "The first metal NiFe (60:40) of a thermocouple is deposited as a 1100 angstrom layer 26 on layer 25 and then first metal layer 26 is patterned with a first mask by ion milling resulting in the layout of FIG. 4d."
4 seep seep seep seep seep seep seep see	depositing and patterning a second metal layer on the nitride layer and the first metal layer for the at least one device;	Column 2 lines 57-60: "For the second metal of the thermocouple detectors, a thousand angstrom layer 27 of chromium is deposited on layers 25 and 26. Layer 27 in FIG. 4e is patterned with a second mask by ion milling and wet etching."
	patterning and removing material from the first wafer and layers on the first side of the first wafer and from a second side of the first wafer to make a pump-out port through the first wafer and the layers on the first wafer;	Column 2 line 68 to column 3 line 1: "Plasma etched vias 32 in FIG 4i for the final etch are patterned and cut with the use of a fifth mask." Column 3 lines 6-11: "Plasma etched pump-out port vias 11 are patterned and cut on layers 23b and 23a of the back of wafer 13 in FIG 4k. There is a KOH etch of the backside of wafer 13 through 90 percent of wafer 13 for port 11 in FIG 4l. Port 11 is completed with an etch through via 32 to the front of wafer 13 as shown in FIG 4m."
	masking and removing material from a first side of a second wafer, to form a recess in the first side of the second wafer;	Column 3 lines 29-31: "Pattern and cut via 35 by plasma etching on outside layers 36a and 36b and recess 16 on inside layer 37b of Si ₃ N ₄ in FIG. 5b." Column 3 lines 35-37: "Wafer 14 is removed from the etching fixture and hole 16 is cleared of remaining SiO ₂ layer 37a in FIG. 5d by buffered oxide etch." Column 3 lines 39-41: "Nitride and oxide mask layers 36a, 36b, 37a, and 37b are stripped from yeafer 14."
	forming a sealing ring on the first side of the second wafer around the recess;	36b, 37a, and 37b are stripped from wafer 14." "A solder ring pattern is applied to the inside surface encircling recess 16, by using a laminated Riston process for lift-off. Five hundred angstroms of Ti, 2000 angstroms of Ni and 500 angstroms of Au of adhesion metals 39 are deposited in an E-beam evaporator. A five micron layer 40 of InPb (10:90) solder is deposited onto adhesion metals 39 in the thermal evaporator. The Riston mask is lifted off and the field SiO.sub.2 in BOE etched off resulting in solder ring 18 in FIG. 5f."

		(Column 3 lines 41-50)
	positioning the first side	
	of the first wafer next to the first side of the second wafer; and	"Wafers 13 and 14 of FIG. 6a are aligned in a bonding cassette using 0.002 inch spacers between the wafers." (Column 3 lines 58-60)
	wherein:	
-	the sealing ring is in contact with at least one of the layers on the first side of the first wafer;	"Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure." (Column 3 lines 62-63)
	the at least one device is within the recess resulting in a chamber containing the at least one device;	In describing Figures 1a, 1b, and 2, "Cavity 16 is the chamber that contains an array 17 of detectors on the surface of wafer 13 and detects radiation which may come through an anti-reflective coated silicon window of top cap 14." (Column 2 lines 17-20.) Further, a plurality of such recesses are shown in Figure 3: "FIG. 3 shows a wafer 20 having multiple chips 10 having a wafer-to-wafer sealing of the same material for multiple cavities." (Column 2 lines 28-30). Further, in describing a nearly finished product, "Wafer 20 may be cut into individual chips 10, each having its own sealed abomber 16 and single that the same was a sealed abomber 16 and single that the same was a sealed abomber 16 and single that the same was a sealed abomber 16 and single that the same was a sealed abomber 16 and single that the same was a sealed abomber 16 and single that the same was a sealed abomber 16 and single that the same was a sealed abomber 16 and single that the same was a sealed abomber 16 and single that the same was a sealed abomber 16 and single that the same was a sealed abomber 16 and single that the same was a sealed abomber 16 and single that the same was a sealed abomber 16 and same was a sealed and same was a sealed abomber 16 and same was a sealed and same was a sealed as a sealed and same was a sea
	the pump-out port is within the sealing ring; and	chamber 16 enclosing detectors 17." (Column 4 lines 15-17) As shown in Figures 1a, 1b, and 2. Also described: "Cavities 16 can be baked out and outgassed since each chamber
	the first and second wafers are effectively a bonded together set of wafers.	"Wafers 13 and 14 are adhered together at a solder seal ring 15." (Column 2 lines 15-16). "The present wafers 13 and 14, after bonding and sealing, may be sawed into individual chips without breakage since the sealed top cap protects the fragile microstructure devices 17. Further, the plug will not be disturbed since it is a deposited layer 12 rather than some dislodgable solder ball or plug." (Column 2 lines 37-42) "The aligned wafer pair is put in a vacuum press which is pumped to a good vacuum with a turbo pump. Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for five minutes. Then wafers 13 and 14 are cooled down to room temperature, and the vacuum chamber is vented. The aligned wafer pair is put in a vacuum press which is pumped to a good vacuum with a turbo pump. Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for five minutes. Then wafers

		13 and 14 are cooled down to room temperature, and the vacuum chamber is vented." (Column 3 lines 60-68). "Bonded wafer pair 13 and 14" (Column 4 line 1) "Then wafers 13 and 14, combined as wafer 20, may be removed from the vacuum environment." (Column 4 lines 13-15).
33	The method of claim 32, further comprising: placing the bonded together set of wafers in an environment of a vacuum wherein a vacuum occurs in the chamber via the pumpout port; and	"Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11. Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 30-34). "Wafer pair 13 and 14 is put into a thermal evaporator system; and a bake out of the wafer pair at 250 degrees C. is preferred for four hours under a vacuum. The wafer pair 13 and 14 is cooled down but the environment about the wafer pair is kept at the desired vacuum. Twenty microns of InPb (50:50) 12 is deposited onto the backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20 scale, a plurality of ports 11 in a plurality of chips are plugged. Then wafers 13 and 14, combined as wafer 20, may be removed from the vacuum environment. Wafer 20 may be cut into individual chips 10, each having its own sealed about the point of the pair of the
	depositing a layer of	chamber 16 enclosing detectors 17." (Column 4 lines 4-17). "Then in an environment of a vacuum, a deposition of metal
	material on the second	12 is applied to the wafer 13 surface having ports 11 and thereby
	side of the first wafer	close ports 11 and seal chambers 16 closed with a vacuum in the
	and the pump-out port	chambers." (Column 2 lines 31-34).
	on the second side of the first wafer, wherein the	"Twenty microns of InPb (50:50) 12 is deposited onto the
	chamber is sealed from	backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal
	the environment.	vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20 scale, a plurality of ports 11 in a plurality of chips are plugged."
		(Column 4 lines 9-13).
34	The method of claim 33,	"Cavities 16 can be baked out and outgassed since each
	further comprising	chamber 16 has an open port 11. Then in an environment of a
	baking out the bonded together set of wafers	vacuum, a deposition of metal 12 is applied to the wafer 13
	prior to depositing the	surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column
	layer of material on the	2 lines 30-34).
	second side of the first	"Wafer pair 13 and 14 is put into a thermal evaporator
	wafer and the pump-out	system; and a bake out of the wafer pair at 250 degrees C. is
	port on the second side of the first wafer.	preferred for four hours under a vacuum." (Column 4 lines 4-7).
35	The method of claim 34,	"The chamber may enclose at least one device such as a
	wherein the at least one	thermoelectric sensor, bolometer, emitter or other kind of
	device is a detector.	device." (Abstract).

		"Each cavity, chamber or volume may contain detectors
		such as thermoelectric detectors, devices, bolometers, or may
		contain emitters." (Column 1 lines 56-58).
		"Cavity 16 is the chamber that contains an array 17 of
-		detectors on the surface of wafer 13 and detects radiation which
		may come through an anti-reflective coated silicon window of
		top cap 14." (Column 2 lines 17-20).
36	The method of claim 35,	"The chamber may enclose at least one device such as a
	wherein the at least one	thermoelectric sensor, bolometer, emitter or other kind of
	device is a	device." (Abstract).
	thermoelectric detector.	"Each cavity, chamber or volume may contain detectors
		such as thermoelectric detectors, devices, bolometers, or may
		contain emitters." (Column 1 lines 56-58).
37	The method of claim 34,	"The chamber may enclose at least one device such as a
	wherein the at least one	thermoelectric sensor, bolometer, emitter or other kind of
	device is an emitter.	device." (Abstract).
İ		"Each cavity, chamber or volume may contain detectors
		such as thermoelectric detectors, devices, bolometers, or may
38	A method for making a	contain emitters." (Column 1 lines 56-58).
130	wafer-pair having sealed	Column 2 line 68 to column 3 line 1: "Plasma etched vias
	chambers, comprising:	32 in FIG 4i for the final etch are patterned and cut with the use
	1	of a fifth mask."
- 8	patterning and removing material from the first	Column 3 lines 6-11: "Plastma etched pump-out port vias
		11 are patterned and cut on layers 23b and 23a of the back of
	wafer to make a	wafer 13 in FIG 4k. There is a KOH etch of the backside of
Ì	plurality of pump-out	wafer 13 through 90 perent of wafer 13 for port 11 in FIG 41.
	ports through the first	Port 11 is completed with an etch through via 32 to the front of
	wafer;	wafer 13 as shown in FIG 4m."
	masking and removing	Column 3 lines 29-31: "Pattern and cut via 35 by plasma
	material from a first side	etching on outside layers 36a and 36b and recess 16 on inside
	of a second wafer to	layer 37b of Si ₃ N ₄ in FIG. 5b."
	form a plurality of	Column 3 lines 35-37: "Wafer 14 is removed from the
	recesses in the first side	etching fixture and hole 16 is cleared of remaining SiO ₂ layer
ļ	of the second wafer;	37a in FIG. 5d by buffered oxide etch."
		Column 3 lines 39-41: "Nitride and oxide mask layers 36a,
		36b, 37a, and 37b are stripped from wafer 14."
	forming a sealing ring	"A solder ring pattern is applied to the inside surface
	on a first side of the first	encircling recess 16, by using a laminated Riston process for lift-
	wafer or the first side of	off. Five hundred angstroms of Ti, 2000 angstroms of Ni and
	the second wafer such	500 angstroms of Au of adhesion metals 39 are deposited in an
	that the sealing ring	E-beam evaporator. A five micron layer 40 of InPb (10:90)
	extends around each of	solder is deposited onto adhesion metals 39 in the thermal
	the plurality of recesses;	evaporator. The Riston mask is lifted off and the field SiO.sub.2
	and	in BOE etched off resulting in solder ring 18 in FIG. 5f."
		(Column 3 lines 41-50). See also Figure 1b where seal ring 15
		extends around recess 16.
		Therefore at Calle 100000 1U.

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positioning the first side of the first wafer next to the first side of the second wafer; and	"Wafers 13 and 14 of FIG. 6a are aligned in a bonding cassette using 0.002 inch spacers between the wafers." (Column 3 lines 58-60)
wherein: each sealing ring is in contact with the first side of the first wafer and the first side of the second wafer	"Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure." (Column 3 lines 62-63)
each recess of the plurality of recesses results in a chamber;	In describing Figures 1a, 1b, and 2, "Cavity 16 is the chamber that contains an array 17 of detectors on the surface of wafer 13 and detects radiation which may come through an anti-reflective coated silicon window of top cap 14." (Column 2 lines 17-20.) Further, a plurality of such recesses are shown in Figure 3: "FIG. 3 shows a wafer 20 having multiple chips 10 having a wafer-to-wafer sealing of the same material for multiple cavities." (Column 2 lines 28-30). Further, in describing a nearly finished product, "Wafer 20 may be cut into individual chips 10, each having its own sealed chamber 16 enclosing detectors 17." (Column 4 lines 15-17)
each sealing ring encloses at least one pump-out port of the plurality of pump-out ports; and	As shown in Figures 1a and 1b. As noted in Column 2 lines 30-31, "Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11." Column 3 lines 42-50 note that a solder ring pattern (a sealing ring) encircles the recess. Column 4 lines 15-17 notes that each chip has its own sealed chamber.
the first and second wafers are effectively a bonded together set of wafers.	"Wafers 13 and 14 are adhered together at a solder seal ring 15." (Column 2 lines 15-16). "The present wafers 13 and 14, after bonding and sealing, may be sawed into individual chips without breakage since the sealed top cap protects the fragile microstructure devices 17. Further, the plug will not be disturbed since it is a deposited layer 12 rather than some dislodgable solder ball or plug." (Column 2 lines 37-42) "The aligned wafer pair is put in a vacuum press which is pumped to a good vacuum with a turbo pump. Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for five minutes. Then wafers 13 and 14 are cooled down to room temperature, and the vacuum chamber is vented. The aligned wafer pair is put in a vacuum press which is pumped to a good vacuum with a turbo pump. Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which

		takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for five minutes. Then wafers 13 and 14 are cooled down to room temperature, and the vacuum chamber is vented." (Column 3 lines 60-68). "Bonded wafer pair 13 and 14" (Column 4 line 1) "Then wafers 13 and 14, combined as wafer 20, may be removed from the vacuum environment." (Column 4 lines 13-15).
39	The method of claim 38,	"Cavities 16 can be baked out and outgassed since each
	further comprising: placing the set of wafers	chamber 16 has an open port 11. Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13
	in an environment of a	surface having ports 11 and thereby close ports 11 and seal
	vacuum wherein a	chambers 16 closed with a vacuum in the chambers." (Column
	vacuum occurs in each	2 lines 30-34).
	chamber via a pump-out	"Wafer pair 13 and 14 is put into a thermal evaporator
	port; and	system; and a bake out of the wafer pair at 250 degrees C. is
		preferred for four hours under a vacuum. The wafer pair 13 and
		14 is cooled down but the environment about the wafer pair is
		kept at the desired vacuum. Twenty microns of InPb (50:50) 12
		is deposited onto the backside of detector wafer 13 to plug port
		11 in FIG. 6c, to seal vacuum chamber 16 of wafer pair 13 and
		14. On the wafer 20 scale, a plurality of ports 11 in a plurality of
		chips are plugged. Then wafers 13 and 14, combined as wafer 20, may be removed from the vacuum environment. Wafer 20
ļ		may be cut into individual chips 10, each having its own sealed
		chamber 16 enclosing detectors 17." (Column 4 lines 4-17).
	depositing a layer of	"Then in an environment of a vacuum, a deposition of metal
	material on a second	12 is applied to the wafer 13 surface having ports 11 and thereby
	side of the first wafer to	close ports 11 and seal chambers 16 closed with a vacuum in the
	seal the plurality of	chambers." (Column 2 lines 31-34).
	pump-out out ports from	"Twenty microns of InPb (50:50) 12 is deposited onto the
	the second side of the	backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal
	first wafer, wherein each	vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20
	chamber is sealed from the environment.	scale, a plurality of ports 11 in a plurality of chips are plugged."
40	The method of claim 39,	(Column 4 lines 9-13).
	further comprising	"Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11. Then in an environment of a
	baking out the set of	vacuum, a deposition of metal 12 is applied to the wafer 13
	wafers prior to	surface having ports 11 and thereby close ports 11 and seal
	depositing the layer of	chambers 16 closed with a vacuum in the chambers." (Column
	material on the second	2 lines 30-34).
	side of the first wafer.	"Wafer pair 13 and 14 is put into a thermal evaporator
		system; and a bake out of the wafer pair at 250 degrees C. is
4.5		preferred for four hours under a vacuum." (Column 4 lines 4-7).
41	The method of claim 40,	"The present wafers 13 and 14, after bonding and sealing,
	wherein the set of	may be sawed into individual chips without breakage since the

		wafers is cut into a plurality of chips wherein each chip has one or more sealed chambers.	sealed top cap protects the fragile microstructure devices 17. Further, the plug will not be disturbed since it is a deposited layer 12 rather than some dislodgable solder ball or plug." (Column 2 lines 37-42). "Wafer 20 may be cut into individual chips 10, each having its own sealed chamber 16 enclosing detectors 17." (Column 4 lines 15-17).
. He all the grind, arrang turns, grind, arrang turns, grind, gri	42	The method of claim 40, wherein the one or more sealed chambers contains one or more devices.	"The procedure here has been implemented and resulted in vacuum levels below 10 millitorr of residual pressure as measured by pressure sensors within the cavity." (Column 1 lines 41-44). "Each cavity, chamber or volume may contain detectors such as thermoelectric detectors, devices, bolometers, or may contain emitters." (Column 1 lines 56-58). "Cavity 16 is the chamber that contains an array 17 of detectors on the surface of wafer 13 and detects radiation which may come through an anti-reflective coated silicon window of top cap 14." (Column 2 lines 17-20). "Wafer 20 may be cut into individual chips 10, each having its own sealed chamber 16 enclosing detectors 17." (Column 4 lines 15-17). "Top cap wafer 14 may have integrated components built in or on the surface in addition to those on the detector wafer 13. Detector wafer 13 having a diaphragm pressure sensor integrated into it, the sealed chamber then forms a vacuum pressure reference. Detector wafer 13 may have infrared bolometer arrays with readout electronics integrated into the wafer. Detector wafer 13 may have moving parts to be sealed in a chamber for other functional purposes." (Column 4 lines 22-30).
gas pak	43	The method of claim 38, further comprising: placing the set of wafers in an environment of a gas wherein the gas enters each chamber via a pump-out port; and depositing a layer of material on a second side of the first wafer to seal the plurality of pump-out out ports from the second side of the first wafer, wherein each chamber is sealed from an ambient environment.	As noted, instead of evacuating the chambers, the chambers may be filled with a gas and sealed. "Each cavity may have a gas instead of a vacuum." (Column 1 lines 55-56). "The bonded wafer pair 13 and 14 in FIG. 6c may be hermetically sealed with a controlled residual pressure of a specific gas type for optimal thermal, mechanical or other properties rather than simply evacuated for the devices within the chamber." (Column 4 lines 30-34). The method for performing this action is similar to that used to create a vacuum, where the chamber is sealed by depositing a layer of material to seal the plurality of pump-out ports: "Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11. Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 31-34). "Twenty microns of InPb (50:50) 12 is deposited onto the

backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20 scale, a plurality of ports 11 in a plurality of chips are plugged." (Column 4 lines 9-13).
"Plasma etched vias 32 in FIG 4i for the final etch are patterned and cut with the use of a fifth mask." (Column 2 line tween, viding a "Plasma etched pump-out port vias 11 are patterned and cut
on layers 23b and 23a of the back of wafer 13 in FIG 4k. There is a KOH etch of the backside of wafer 13 through 90 percent of wafer 13 for port 11 in FIG 4l. Port 11 is completed with an etch through via 32 to the front of wafer 13 as shown in FIG 4m." (Column 3 lines 6-11).
st side "A solder ring pattern is applied to the inside surface encircling recess 16, by using a laminated Riston process for lift-
off. Five hundred angstroms of Ti, 2000 angstroms of Ni and
ling ring 500 angstroms of Au of adhesion metals 39 are deposited in an E-beam evaporator. A five micron layer 40 of InPb (10:90)
solder is deposited onto adhesion metals 39 in the thermal
evaporator. The Riston mask is lifted off and the field SiO.sub.2 in BOE etched off resulting in solder ring 18 in FIG. 5f."
(Column 3 lines 41-50). "Wafers 13 and 14 of FIG. 6a are aligned in a bonding
cassette using 0.002 inch spacers between the wafers." (Column 3 lines 58-60).
the 36a and 36b and recess 16 on inside layer 37b of Si ₂ N ₄ in FIG
5b." (Column 3 lines 29-31). "Wafer 14 is removed from the etching fixture and hole 16
is cleared of remaining SiO ₂ layer 37a in FIG. 5d by buffered oxide etch." (Column 3 lines 35-37).
"Nitride and oxide mask layers 36a, 36b, 37a, and 37b are stripped from wafer 14." (Column 3 lines 39-41).
"A solder ring pattern is applied to the inside surface encircling recess 16, by using a laminated Riston process for lift-
off. Five hundred angstroms of Ti, 2000 angstroms of Ni and
500 angstroms of Au of adhesion metals 39 are deposited in an E-beam evaporator. A five micron layer 40 of InPb (10:90)
solder is deposited onto adhesion metals 39 in the thermal
evaporator. The Riston mask is lifted off and the field SiO.sub.2 in BOE etched off resulting in solder ring 18 in FIG. 5f."
(Column 3 lines 41-50). "Wafers 13 and 14 are pressed together in FIG. 6b, with
about 400 pounds of pressure." (Column 3 lines 62-63).
t port "Cavities 16 can be baked out and outgassed since each
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	communication with the	And also at the property of
·	chamber; and	And also as shown in Figure 6b.
	plugging the pump out port to seal the chamber.	"Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 31-34). "Twenty microns of InPb (50:50) 12 is deposited onto the backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20 scale, a plurality of ports 11 in a plurality of chips are plugged." (Column 4 lines 9-13).
	A method according to claim 44 further comprising the step of: making a recess in the first side of the first wafer and/or the first side of the second wafer, wherein the recess is in registration with the chamber.	"Pattern and cut via 35 by plasma etching on outside layers 36a and 36b and recess 16 on inside layer 37b of Si ₃ N ₄ in FIG. 5b." (Column 3 lines 29-31). "Wafer 14 is removed from the etching fixture and hole 16 is cleared of remaining SiO ₂ layer 37a in FIG. 5d by buffered oxide etch." (Column 3 lines 35-37). "Nitride and oxide mask layers 36a, 36b, 37a, and 37b are stripped from wafer 14." (Column 3 lines 39-41).
46	A method according to claim 44 further comprising the step of: providing one or more devices in or on the first side of the first wafer and/or the first side of the second wafer before the positioning step.	The first metal NiFe (60:40) of a thermocouple is deposited as a 1100 angstrom layer 26 on layer 25 and then first metal layer 26 is patterned with a first mask by ion milling resulting in the layout of FIG. 4d. For the second metal of the thermocouple detectors, a thousand angstrom layer 27 of chromium is deposited on layers 25 and 26. Layer 27 in FIG. 4e is patterned with a second mask by ion milling and wet etching. A layer 28 consisting of 6000 angstroms of Si.sub.3 N.sub.4 is deposited on metal layers 26 and 27, and layer 25, as the top bridge nitride in FIG. 4f. An absorber 29 is deposited on layer 28 of FIG. 4g and patterned with a third mask. Absorber 29 is capped with a layer 30 of Si.sub.3 N.sub.4. Plasma etched vias 31 to metal layer 27 are patterned and cut with the use of a fourth mask, as shown in FIG. 4h. Plasma etched vias 32 in FIG. 4i for the final etch are patterned and cut with the use of a fifth mask. Five hundred angstroms of Cr, 2000 angstroms of Ni and 5000 angstroms of Au are deposited, patterned and lifted off for pad and solder frame metal 33 in FIG. 4j. Passivated leadouts 40 in first metal 26 or second metal 27 pass under the seal ring metal 33 in FIG. 4j. Plasma etched pump-out port vias 11 are patterned and cut on layers 23b and 23a of the back of wafer 13 in FIG. 4k. There is a KOH etch of the back side of wafer 13 through 90 percent of wafer 13 for port 11 in FIG. 4l. Port 11 is completed with an etch through via 32 to the front of wafer 13 as shown in FIG.

		4 (0.1 0.11
47	A	4m. (Column 2 line 53 to column 3 line 11).
4/	A method according to	"The procedure here has been implemented and resulted in
	claim 46 wherein the	vacuum levels below 10 millitorr of residual pressure as
1	one or more devices are	measured by pressure sensors within the cavity." (Column 1
	in registration with the chamber.	lines 41-44).
	Chamber.	"Each cavity, chamber or volume may contain detectors
		such as thermoelectric detectors, devices, bolometers, or may
		contain emitters." (Column 1 lines 56-58).
		"Cavity 16 is the chamber that contains an array 17 of
		detectors on the surface of wafer 13 and detects radiation which
		may come through an anti-reflective coated silicon window of
		top cap 14." (Column 2 lines 17-20).
		"Wafer 20 may be cut into individual chips 10, each having
		its own sealed chamber 16 enclosing detectors 17." (Column 4
		lines 15-17).
		"Top cap wafer 14 may have integrated components built in
		or on the surface in addition to those on the detector wafer 13.
		Detector wafer 13 having a diaphragm pressure sensor integrated
		into it, the sealed chamber then forms a vacuum pressure
		reference. Detector wafer 13 may have infrared bolometer arrays
		with readout electronics integrated into the wafer. Detector
		wafer 13 may have moving parts to be sealed in a chamber for other functional purposes." (Column 4 lines 22-30).
48	A method for making a	"Plasma etched vias 32 in FIG 4i for the final etch are
	wafer-pair with a sealed	patterned and cut with the use of a fifth mask." (Column 2 line
	chamber therebetween,	68 to column 3 line 1).
	comprising: providing a	"Plasma etched pump-out port vias 11 are patterned and cut
	first wafer and a second	on layers 23b and 23a of the back of wafer 13 in FIG 4k. There
	wafer; forming one or	is a KOH etch of the backside of wafer 13 through 90 percent of
	more pump-out ports	wafer 13 for port 11 in FIG 41. Port 11 is completed with an
	through the first wafer;	etch through via 32 to the front of wafer 13 as shown in FIG
		4m." (Column 3 lines 6-11).
48b	making a recess in a first	"Pattern and cut via 35 by plasma etching on outside layers
	side of the first wafer	36a and 36b and recess 16 on inside layer 37b of Si ₃ N ₄ in FIG.
	and/or a first side of the	5b." (Column 3 lines 29-31).
	second wafer;	"Wafer 14 is removed from the etching fixture and hole 16
		is cleared of remaining SiO ₂ layer 37a in FIG. 5d by buffered
		oxide etch." (Column 3 lines 35-37).
	1.	"Nitride and oxide mask layers 36a, 36b, 37a, and 37b are
- ·	positioning the first side	stripped from wafer 14." (Column 3 lines 39-41).
	of the first wafer next to	"Wafers 13 and 14 of FIG. 6a are aligned in a bonding
	the first side of the	cassette using 0.002 inch spacers between the wafers." (Column 3 lines 58-60).
	second wafer,	5 mies 56-00).
	the first wafer and the	"Cavity 16 is affected by a record of 1 125
	second wafer forming a	"Cavity 16 is effected by a recess of about 125 microns into
	, orde mater forming a	wafer 14 having a border 18." (Column 2 lines 21-22).

		1 1 1 1	
		chamber that is at least	
		partially defined by the	
		recess,	
		with the pump-out port	"Cavities 16 can be baked out and outgassed since each
		of the first wafer in fluid	chamber 16 has an open port 11." Column 2 lines 30-31. Fluid
		communication with the	communication of the pump-out port of the first wafer with the
		chamber; and	chamber is also shown in Figure 6b.
		plugging the pump out	"Then in an environment of a vacuum, a deposition of metal
		port to seal the chamber.	12 is applied to the wafer 13 surface having ports 11 and thereby
			close ports 11 and seal chambers 16 closed with a vacuum in the
			chambers." (Column 2 lines 31-34).
			"Twenty microns of InPb (50:50) 12 is deposited onto the
			backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal
			vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20
			scale a physolity of ports 11 in a physolity of china and 11
			scale, a plurality of ports 11 in a plurality of chips are plugged." (Column 4 lines 9-13).
	49	A method for making a	
	77	wafer-pair with a sealed	As shown in Figure 4j and also discussed in the
İ		chamber therebetween,	specification: "Five hundred angstroms of Cr, 2000 angstroms
			of Ni and 5000 angstroms of Au are deposited, patterned and
		comprising: providing a	lifted off for pad and solder frame metal 33 in FIG. 4j."
		first wafer having a first	(Column 3 lines 1-4).
		side, with one or more	
		bond pads on the first	
-	н	side;	
1		providing a second	"Pattern and cut via 35 by plasma etching on outside layers
		wafer; forming one or	36a and 36b and recess 16 on inside layer 37b of Si.sub.3
		more bond-pad holes	N.sub.4 in FIG. 5b. The wafer 14 is then put in a fixture to allow
		through the second	etching of the outside surface 35 and 36b while protecting the
		wafer;	inside 16 and 37b to KOH etch wafer 14 through hole 35 to 90
			percent of the way through top cap wafer 14, as shown in FIG.
			5c. Wafer 14 is removed from the etching fixture and hole 16 is
			cleared of remaining SiO2 layer 37a in FIG. 5d by buffered
			oxide etch. Hole 35 is further etched through wafer 14 to layer
L			37a to complete bond pad hole 35." (Column 3 lines 29-39).
		positioning the first side	"A solder ring pattern is applied to the inside surface
		of the first wafer next to	encircling recess 16, by using a laminated Riston process for lift-
		a first side of the second	off. Five hundred angstroms of Ti, 2000 angstroms of Ni and
İ		wafer with a sealing ring	500 angstroms of Au of adhesion metals 39 are deposited in an
		therebetween;	E-beam evaporator. A five micron layer 40 of InPb (10:90)
		-	solder is deposited onto adhesion metals 39 in the thermal
			evaporator. The Riston mask is lifted off and the field SiO.sub.2
			in BOE etched off resulting in solder ring 18 in FIG. 5f."
1	ļ		(Column 3 lines 41-50).
			"Wafers 13 and 14 of FIG. 6a are aligned in a bonding
			cassette using 0.002 inch spacers between the wafers." (Column
			3 lines 58-60).
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the first wafer, the second wafer and the sealing ring forming a chamber,	"Wafer 14 has a solder adhesion metal and solder ring 15 which matches detector wafer 13, a border 18 forming chamber 16 above detectors 17, and holes 35 through wafer 14 to access the wire bond pads on detector wafer 13." (Column 3 lines 19-23).
	"A solder ring pattern is applied to the inside surface encircling recess 16, by using a laminated Riston process for lift-off. Five hundred angstroms of Ti, 2000 angstroms of Ni and 500 angstroms of Au of adhesion metals 39 are deposited in an E-beam evaporator. A five micron layer 40 of InPb (10:90) solder is deposited onto adhesion metals 39 in the thermal evaporator. The Riston mask is lifted off and the field SiO.sub.2 in BOE etched off resulting in solder ring 18 in FIG. 5f." (Column 3 lines 41-50).
	"Pattern and cut via 35 by plasma etching on outside layers 36a and 36b and recess 16 on inside layer 37b of Si ₃ N ₄ in FIG. 5b." (Column 3 lines 29-31).
	"Wafer 14 is removed from the etching fixture and hole 16 is cleared of remaining SiO ₂ layer 37a in FIG. 5d by buffered oxide etch." (Column 3 lines 35-37).
	"Nitride and oxide mask layers 36a, 36b, 37a, and 37b are stripped from wafer 14." (Column 3 lines 39-41).
	Having shown how the sealing ring may be formed for one embodiment, Figures 6a-6c show that the two wafers may be pressed together and the wafers 13, 14 and sealing ring 18 form
the first wafer and	a chamber 16. "Wafer 14 has a solder adhesion metal and solder ring 15
second wafer being aligned so that the bond- pad holes are in registration with the one	which matches detector wafer 13, a border 18 forming chamber 16 above detectors 17, and holes 35 through wafer 14 to access the wire bond pads on detector wafer 13." (Column 3 lines 19-23).
or more bond pads on the first wafer; and	Figures 6a-6c show that the bond pad hole 35 is aligned with bond pad 33. Particularly, Figure 6a numbers more portions of the bond pads 33, and the bond pads 33 are clearly in registration with the bond pad hole 35, though the reference numerals on some of the bond pads 33 are not included in each of the Figures.
the first and second wafers are effectively a bonded together set of wafers.	"Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for five minutes. Then wafers 13 and 14 are cooled down to room temperature, and the vacuum chamber is vented. Bonded wafer pair 13 and 14 is put into an E-beam evaporation system for sputter cleaning of the pump-out port 11
	surfaces, followed by adhesion layers of 500 angstroms of Ti,

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The state of the s			and 14 is put into a thermal evaporator system; and a bake out of the wafer pair at 250 degrees C. is preferred for four hours under a vacuum. The wafer pair 13 and 14 is cooled down but the environment about the wafer pair is kept at the desired vacuum. Twenty microns of InPb (50:50) 12 is deposited onto the backside of detector wafer 13 to plug port 11 in FIG. 6c, to seal vacuum chamber 16 of wafer pair 13 and 14. On the wafer 20 scale, a plurality of ports 11 in a plurality of chips are plugged. Then wafers 13 and 14, combined as wafer 20, may be removed from the vacuum environment." (Column 3 line 60 to column 4 line 15).
The second secon	50	A bonded wafer pair, comprising: a first wafer; a second wafer; the first wafer having one or more pump-out ports through the first wafer;	"Plasma etched vias 32 in FIG 4i for the final etch are patterned and cut with the use of a fifth mask." (Column 2 line 68 to column 3 line 1). "Plasma etched pump-out port vias 11 are patterned and cut on layers 23b and 23a of the back of wafer 13 in FIG 4k. There is a KOH etch of the backside of wafer 13 through 90 percent of wafer 13 for port 11 in FIG 4l. Port 11 is completed with an
			etch through via 32 to the front of wafer 13 as shown in FIG
		the first side of the first wafer bonded to a first side of the second wafer via a sealing ring;	4m." (Column 3 lines 6-11). "Wafers 13 and 14 are bonded together at solder seal ring 15." (Column 2 lines 15-16). "To begin, the Au solder ring surface 33 of detector wafer 13 is sputter cleaned. The InPb surface of ring 18 of top cap wafer 14 is oxygen plasma cleaned. Wafers 13 and 14 of FIG. 6a are aligned in a bonding cassette using 0.002 inch spacers between the wafers. The aligned wafer pair is put in a vacuum press which is pumped to a good vacuum with a turbo pump. Wafers 13 and 14 are pressed together in FIG. 6b, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for five minutes. Then wafers 13 and 14 are cooled down to room temperature, and the vacuum chamber is vented." (Column 3 lines 56-67).
		the first wafer, the second wafer and the sealing ring forming a chamber,	"A solder ring pattern is applied to the inside surface encircling recess 16, by using a laminated Riston process for lift-off. Five hundred angstroms of Ti, 2000 angstroms of Ni and 500 angstroms of Au of adhesion metals 39 are deposited in an E-beam evaporator. A five micron layer 40 of InPb (10:90) solder is deposited onto adhesion metals 39 in the thermal evaporator. The Riston mask is lifted off and the field SiO.sub.2 in BOE etched off resulting in solder ring 18 in FIG. 5f." (Column 3 lines 41-50). "Pattern and cut via 35 by plasma etching on outside layers

		36a and 36b and recess 16 on inside layer 37b of Si ₃ N ₄ in FIG. 5b." (Column 3 lines 29-31).
		"Wafer 14 is removed from the etching fixture and hole 16
İ		is cleared of remaining SiO layer 270 in EIC 54 last layer 1
1		is cleared of remaining SiO ₂ layer 37a in FIG. 5d by buffered
		oxide etch." (Column 3 lines 35-37).
		"Nitride and oxide mask layers 36a, 36b, 37a, and 37b are
		stripped from wafer 14." (Column 3 lines 39-41).
		Having shown how the sealing ring may be formed for one
		embodiment, Figures 6a-6c show that the two wafers may be
		pressed together and the wafers 13, 14 and sealing ring 18 form
		a chamber <u>16</u> .
	with the pump-out port	"Cavities 16 can be baked out and outgassed since each
	of the first wafer in fluid	chamber 16 has an open port 11." (Column 2 lines 30-31).
	communication with the	Fluid communication of the pump-out port of the first wafer
	chamber; and	with the chamber is also shown in Figure 6b.
	a plug for plugging the	"Then in an environment of a vacuum, a deposition of metal
	pump out port.	12 is applied to the wafer 13 surface having ports 11 and thereby
		close ports 11 and seal chambers 16 closed with a vacuum in the
		chambers." (Column 2 lines 31-34).
		"Twenty microns of InPb (50:50) 12 is deposited onto the
		backside of detector wafer 13 to plug port 11 in FIG 6c, to seal
		vacuum chamber 16 of wafer pair 13 and 14." (Column 4 lines
		9-12).
51	A bonded wafer pair	"Cavity 16 is effected by a recess of about 125 microns into
	according to claim 50	wafer 14 having a border 18." (Column 2 lines 21-22).
	further comprising a	"Wafer 14 has a solder adhesion metal and solder ring 15
	recess in the first side of	which matches detector wafer 13, a border 18 forming chamber
	the first wafer and/or the	16 above detectors 17, and holes 35 through wafer 14 to access
	first side of the second	the wire bond pads on detector wafer 13." (Column 3 lines 19-
	wafer, wherein the	23).
	recess is in registration	1
	with the chamber.	
52	A bonded wafer pair	"The procedure here has been implemented and resulted in
	according to claim 50	vacuum levels below 10 millitorr of residual pressure as
	further comprising one	measured by pressure sensors within the cavity." (Column 1
	or more devices in or on	lines 41-44).
	the first side of the first	,
	wafer and/or the first	"Each cavity, chamber or volume may contain detectors
	side of the second wafer.	such as thermoelectric detectors, devices, bolometers, or may
	side of the second water.	contain emitters." (Column 1 lines 56-58).
		"Cavity 16 is the chamber that contains an array 17 of
		detectors on the surface of wafer 13 and detects radiation which
1	,	may come through an anti-reflective coated silicon window of
1		
		top cap 14." (Column 2 lines 17-20).
		top cap 14." (Column 2 lines 17-20). "Wafer 20 may be cut into individual chips 10, each having
		top cap 14." (Column 2 lines 17-20).

	T	(m)
-		"Top cap wafer 14 may have integrated components built in
		or on the surface in addition to those on the detector wafer 13.
		Detector wafer 13 having a diaphragm pressure sensor integrated
		into it, the sealed chamber then forms a vacuum pressure
		reference. Detector wafer 13 may have infrared bolometer arrays
		with readout electronics integrated into the wafer. Detector
		wafer 13 may have moving parts to be sealed in a chamber for
		other functional purposes." (Column 4 lines 22-30).
53	A bonded wafer pair	"The procedure here has been implemented and resulted in
	according to claim 52	vacuum levels below 10 millitorr of residual pressure as
	wherein the one or more	measured by pressure sensors within the cavity." (Column 1
	devices are in	lines 41-44).
	registration with the	"Each cavity, chamber or volume may contain detectors
	chamber.	such as thermoelectric detectors, devices, bolometers, or may
		contain emitters." (Column 1 lines 56-58).
		"Cavity 16 is the chamber that contains an array 17 of
		detectors on the surface of wafer 13 and detects radiation which
		may come through an anti-reflective coated silicon window of
		top cap 14." (Column 2 lines 17-20).
ļ		"Wafer 20 may be cut into individual chips 10, each having
		its own sealed chamber 16 enclosing detectors 17." (Column 4
		lines 15-17). "Top one wefor 14 may have interested common and built in
		"Top cap wafer 14 may have integrated components built in
		or on the surface in addition to those on the detector wafer 13.
		Detector wafer 13 having a diaphragm pressure sensor integrated
		into it, the sealed chamber then forms a vacuum pressure
		reference. Detector wafer 13 may have infrared bolometer arrays
		with readout electronics integrated into the wafer. Detector
		wafer 13 may have moving parts to be sealed in a chamber for
<u> </u>	A 1 1 . 1 C	other functional purposes." (Column 4 lines 22-30).
54	A bonded wafer pair	"Wafers 13 and 14 are bonded together at solder seal ring
	having a sealed	15." (Column 2 lines 15-16).
	chamber, comprising: a	"To begin, the Au solder ring surface 33 of detector wafer
	first wafer; a second	13 is sputter cleaned. The InPb surface of ring 18 of top cap
	wafer bonded to the first	wafer 14 is oxygen plasma cleaned. Wafers 13 and 14 of FIG. 6a
	wafer;	are aligned in a bonding cassette using 0.002 inch spacers
		between the wafers. The aligned wafer pair is put in a vacuum
		press which is pumped to a good vacuum with a turbo pump.
		Wafers 13 and 14 are pressed together in FIG. 6b, with about
		400 pounds of pressure. The temperature of the wafers is ramped
		up to 300 degrees C., which takes about one hour. Then wafers
		13 and 14 are held at this achieved temperature and pressure for
		five minutes. Then wafers 13 and 14 are cooled down to room
		temperature, and the vacuum chamber is vented." (Column 3
		lines 56-67).
	one or more pump-out	"Plasma etched vias 32 in FIG 4i for the final etch are

	ports through the first wafer; a recess in a first side of the first wafer and/or a first side of the second	patterned and cut with the use of a fifth mask." (Column 2 line 68 to column 3 line 1). "Plasma etched pump-out port vias 11 are patterned and cut on layers 23b and 23a of the back of wafer 13 in FIG 4k. There is a KOH etch of the backside of wafer 13 through 90 percent of wafer 13 for port 11 in FIG 4l. Port 11 is completed with an etch through via 32 to the front of wafer 13 as shown in FIG 4m." (Column 3 lines 6-11). A recess is shown cut into wafer 14 in Figures 5c-5f.
	wafer; the first wafer and the second wafer forming a chamber that includes the recess,	"Cavity 16 is effected by a recess of about 125 microns into wafer 14 having a border 18." (Column 2 lines 21-22). "Wafer 14 has a solder adhesion metal and solder ring 15 which matches detector wafer 13, a border 18 forming chamber 16 above detectors 17, and holes 35 through wafer 14 to access the wire bond pads on detector wafer 13." (Column 3 lines 19-23).
	with the pump-out port of the first wafer in fluid communication with the chamber; and one or more plugs for plugging the one or more pump out ports to seal the chamber.	A chamber including the recess 16 is shown in Figures 6a-c. "Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11." (Column 2 lines 30-31). Fluid communication of the pump-out port of the first wafer with the chamber is also shown in Figure 6b. "Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers." (Column 2 lines 31-34). "Twenty microns of InPb (50:50) 12 is deposited onto the backside of detector wafer 13 to plug port 11 in FIG 6c, to seal vacuum chamber 16 of wafer pair 13 and 14." (Column 4 lines 0.12)
55	A bonded wafer pair, comprising: a first wafer having a first side, with one or more bond pads on the first side; a second wafer, with one or more bond-pad holes through the second wafer;	As shown in Figure 4j and also discussed in the specification: "Five hundred angstroms of Cr, 2000 angstroms of Ni and 5000 angstroms of Au are deposited, patterned and lifted off for pad and solder frame metal 33 in FIG. 4j." (Column 3 lines 1-4). "Pattern and cut via 35 by plasma etching on outside layers 36a and 36b and recess 16 on inside layer 37b of Si.sub.3 N.sub.4 in FIG. 5b. The wafer 14 is then put in a fixture to allow etching of the outside surface 35 and 36b while protecting the inside 16 and 37b to KOH etch wafer 14 through hole 35 to 90 percent of the way through top cap wafer 14, as shown in FIG. 5c. Wafer 14 is removed from the etching fixture and hole 16 is cleared of remaining SiO2 layer 37a in FIG. 5d by buffered oxide etch. Hole 35 is further etched through wafer 14 to layer

	37a to complete bond pad hole 35." (Column 3 lines 29-39).
the first side of the first	"Wafers 13 and 14 are bonded together at solder seal ring
wafer bonded to a first	15." (Column 2 lines 15-16).
side of the second wafer	"To begin, the Au solder ring surface 33 of detector wafer
with a sealing ring	13 is sputter cleaned. The InPb surface of ring 18 of top cap
therebetween,	wafer 14 is oxygen plasma cleaned. Wafers 13 and 14 of FIG. 6a
	are aligned in a bonding cassette using 0.002 inch spacers
	between the wafers. The aligned wafer pair is put in a vacuum
	press which is pumped to a good vacuum with a turbo pump.
	Wafers 13 and 14 are pressed together in FIG. 6b, with about
	400 pounds of pressure. The temperature of the wafers is ramped
	up to 300 degrees C., which takes about one hour. Then wafers 13 and 14 are held at this achieved temperature and pressure for
	five minutes. Then wafers 13 and 14 are cooled down to room
	temperature, and the vacuum chamber is vented." (Column 3)
	lines 56-67).
the first wafer and	Figures 6a-6c show that the bond pad hole 35 is aligned
second wafer being	with bond pad 33. Particularly, Figure 6a numbers more
aligned so that the bond-	portions of the bond pads 33, and the bond pads 33 are clearly in
pad holes are in	registration with the bond pad hole 35, though the reference
registration with the one	numerals on some of the bond pads 33 are not included in each
or more bond pads on the first wafer; and	of the Figures.
the first wafer, the	"Wafer 14 has a solder adhesion metal and solder ring 15
second wafer and the	which matches detector wafer 13, a border 18 forming chamber
sealing ring forming a	16 above detectors 17, and holes 35 through wafer 14 to access
chamber.	the wire bond pads on detector wafer 13." (Column 3 lines 19-23).
	"A solder ring pattern is applied to the inside surface
	encircling recess 16, by using a laminated Riston process for lift-
	off. Five hundred angstroms of Ti, 2000 angstroms of Ni and
	500 angstroms of Au of adhesion metals 39 are deposited in an
	E-beam evaporator. A five micron layer 40 of InPb (10:90)
	solder is deposited onto adhesion metals 39 in the thermal
	evaporator. The Riston mask is lifted off and the field SiO.sub.2
	in BOE etched off resulting in solder ring 18 in FIG. 5f."
	(Column 3 lines 41-50).
	"Pattern and cut via 35 by plasma etching on outside layers
	36a and 36b and recess 16 on inside layer 37b of Si ₃ N ₄ in FIG. 5b." (Column 3 lines 29-31).
	"Wafer 14 is removed from the etching fixture and hole 16
	is cleared of remaining SiO ₂ layer 37a in FIG. 5d by buffered
	oxide etch." (Column 3 lines 35-37).
	"Nitride and oxide mask layers 36a, 36b, 37a, and 37b are
	stripped from wafer 14." (Column 3 lines 39-41).
	Having shown how the sealing ring may be formed for one

embodiment, Figures 6a-6c show that the two wafers may be pressed together and the wafers 13, 14 and sealing ring 18 form a chamber 16.

Respectfully submitted,

R. Andrew Wood et al.

By their attorney,

Date: DumBGL 3, 2001

Brian N. Tufte, Reg. No. 38,638

CROMPTON, SEAGER & TUFTE, LLC

331 Second Avenue South, Suite 895

Minneapolis, Minnesota 55401-2246

Telephone:

(612) 677-9050

Facsimile:

(612) 359-9349